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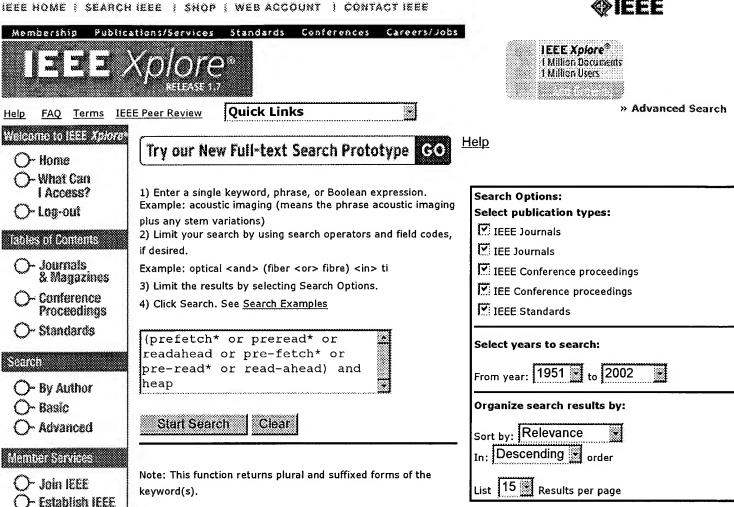
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1 Avoiding initialization misses to the heap

Lewis, J.A.; Black, B.; Lipasti, M.H.;

Computer Architecture, 2002. Proceedings. 29th Annual International Symposium on , 25-29 May 2002

Pages: 183 - 194

[Abstract]

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2 Page fault behavior and two prepaging schemes

Seongje Cho; Yookun Cho;

Computers and Communications, 1996., Conference Proceedings of the 1996 IEEE Fifteenth Annual International Phoenix Conference on , 27-29 March 1996

Pages: 15 - 21

[Abstract] [PDF Full-Text (668 KB)] IEEE CNI

3 Supporting high level programming with high performance: the Illinois Concert system

Chien, A.; Dolby, J.; Ganguly, B.; Karamcheti, V.; Xingbin Zhang; High-Level Programming Models and Supportive Environments, 1997. Proceedings., Second International Workshop on, 1 April 1997

Pages: 15 - 24

[Abstract] [PDF Full-Text (848 KB)] IEEE CNF

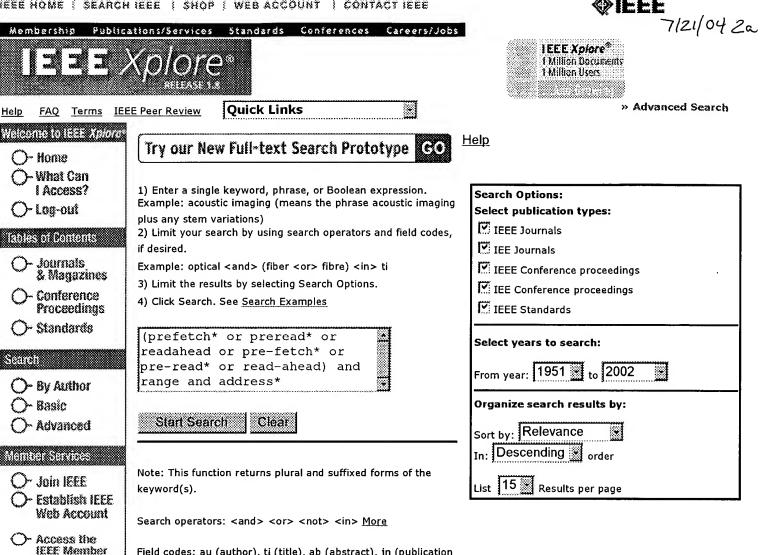
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Chien, A.; Dolby, J.; Ganguly, B.; Karamcheti, V.; Xingbin Zhang; High-Level Programming Models and Supportive Environments, 1997. Proceedings., Second International Workshop on , 1 April 1997 Pages:15 - 24

[Abstract] [PDF Full-Text (848 KB)] IEEE CNF

2 Data prefetching by dependence graph precomputation

Annavaram, M.; Patel, J.M.; Davidson, E.S.;

Computer Architecture, 2001. Proceedings. 28th Annual International Symposium on , 30 June-4 July 2001

Pages:52 - 61

[PDF Full-Text (176 KB)] [Abstract] TEEE CNE

3 Sunder: a programmable hardware prefetch architecture for numerical loops

Tzi-cker Chiueh;

Supercomputing '94. Proceedings, 14-18 Nov. 1994

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[PDF Full-Text (764 KB)] [Abstract]

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14	17	(speculativ\$3 near2 (read\$3 or fetch\$3 or	USPAT;	2004/07/21
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		(read\$3 or fetch\$3 or load\$3))	US-PGPUB;	15:23
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